

ADFP Cloud 2.0

Full-custom 設計使用者手冊 2024.11.18 Version 1

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ADFP Cloud 2.0	1
1. ADFP Cloud 2.0 PDK 下載與安裝	3
2. Circuit Design (Schematic)	6
3. Pre-Layout Simulation	9
4. Layout	15
5. Layout Verification – DRC	16
6. Layout Verification – LVS	20
7. Layout Verification – PEX	24
8. Post-Layout Simulation	30
9. 查看 TSMC 提供之 FC 文件範例練習	35
10. 查看 NYCU 課程提供之 FC 文件範例練習	
Revision Record and Author List	37



1. ADFP Cloud 2.0 PDK 下載與安裝

1.1 拷貝製程資料夾

目標資料夾: /ADFP/Executable_Package/Collaterals/Tech/iPDK/N16ADFP_iPDK/

[~]\$ cd ~

[~]\$ mkdir ADFP

[~]\$ cd ADFP

[~/ADFP]\$ cp -r /ADFP/Executable_Package/Collaterals/Tech/iPDK/N16ADFP_iPDK/.

DING! vlsi_labTA01@cad11[~]\$ cd ~ 15:01 vlsi_labTA01@cad11[~]\$ mkdir ADFP 15:02 vlsi_labTA01@cad11[~/ADFP]\$ cp -r /ADFP/Executable_Package/Collaterals/Tech/iPDK/N16ADFP_iPDK/ . 15:04 vlsi_labTA01@cad11[~/ADFP]\$ cd N16ADFP_iPDK/ 15:09 vlsi_labTA01@cad11[~/ADFP/N16ADFP_iPDK]\$./p pdkInstall.cfg* pdkInstall.pl* 15:09 vlsi_labTA01@cad11[~/ADFP/N16ADFP_iPDK]\$./pdkInstall.pl

1.2 安裝 PDK (必要步驟)

於該資料夾中執行 ./pdkInstall.pl,並依序輸入 「2, 1, 1, 1, y」

[~/ADFP]\$ cd N16ADFP_iPDK

[~/ADFP/N16ADFP_iPDK]\$./pdkInstall.pl

- TSMC Process Desig	n Kit (PDK) Insta	l Utility -	
Please enter your choice: (2	1/2) :		
Please enter your choice: (1	1,2)		
Please enter your choice: (1,2)		
⊥			
Please enter your choice: (1,2)		
1			
tersenere a service de la construction de la construction de la construction de la construction de la construct	*****	****	
Are these correct (y n) ?			



1.3 確認是否正確完成安裝

出現以下畫面代表成功安裝

```
*Info: PDK installation completed.
15:13 vlsi_labTA01@cad11[~/ADFP/N16ADFP_iPDK]$
```

1.4 創建並修改.cdsinit 檔案

(1) 在 N16ADFP_iPDK 資料中,新增「.cdsinit」檔案





(2) Show hidden file to find ".cdsinit"



(3) 打開檔案並加入以下文字,這會讓 Calibre 加入 Virtuoso 畫面中

;Set Calibre Path

load(strcat(getShellEnvVar("MGC_HOME") "/lib/calibre.OA.skl"))



(3) Add text into ".cdsinit" This step is to add Calibre Interface into Virtuoso

- 1.5 安裝完成^w^
- 1.6 在這個範例教程,將會使用以下 EDA 工具作為教學





2. Circuit Design (Schematic)



* Do This Step Before Using Any Tool



2.2 打開 Virtuoso 軟體

[~/ADFP/N16ADFP_iPDK]\$ virtuoso &



請注意,打開的版本為 ICADVM,而非 IC6。

2.3 創建 Library

(1)點選「Tool」→ 「Library Manager」

(2)點選「File」→「New」→「Library」

			Library Manager: Directory URS	SE/vlsi_lab/vlsi_lab	TA01/C18@	ee31 -	- 🗆 X
			File Edit View Design Manager	Help			cādence
		<	<u>N</u> ew	📫 Library	Ctrl+N	\triangleright	
			🖻 Open Car+o	Sen Menter	Ctrl+N	v	
			Open (<u>R</u> ead-Only) Ctrl+R	C <u>a</u> tegory	Ctrl+N		•
VirtuosoR 6.1.8-64b - Log: /RAID2	/COURSE/vlsi_lab/vlsi_labTA01/CDS.log@ee31		Copen With		- Ba		•
File Tools Options Help			<u>1</u> inv inv schematic			View 🛆 Loc	k Size
			Load Defaults	N			
Libe Library Manager	D		Save Defaults	APS			
	ment"		Open Shell Window Ctrl+P				
"The	n environment has completed."		Exit Ctrl+X				
"The SystemVerilog	ackground."						
INFO <u>N</u> C-Verilog	schematic"		N_U	V_33			
INFO VHDL Toolbox	completed with no errors.			ERO 18			
ADE Assembler	tic" saved.		Messages			-1	
ADE Explorer			Created new library "inv" at /RAID2/C	OURSE/vlsi_lab/vls	i_labTA01/C	18/inv.	
						-	
ADE Veritier	M: schHiSaveAs()		-				
ADE L	mschillsuvchs()			100			
			New Library			Lib: CIC_	Lib Free: 120.09T

(1) Tools -> Library Manager

(2) File -> New -> Library



(3) 輸入 Library Name (這邊以輸入 "Lab" 示範)

(4) 點選「Attach to an existing technology library」→ 「OK」

```
(5)點選「tsmcN16」→ 「OK」
```



2.5 Create Inverter Schematic / Symbol Design

請根據自行需求繪製 Schematic / Symbol



3. Pre-Layout Simulation







(1) 選擇需要輸出德 Library 和 Cell (可使用 Library Browser)

(2) 輸入 output netlist 名字,例如 inv.cir

(3)點選「OK」

r	CDL Out	×		
Template File	Browse Load	Save		
Design to be Netlisted				
Library Name	Lab	Library Browser		
Top Cell Name	inv			
View Name	schematic		1	
Switch View List	auCdl schematic			
Stop View List	auCd1			
COutput	\frown			
Output CDL Netlist File	inv.cir	View		
Run Directory		Browse		
Netlisting Mode	Digital Analog			
Run in Background	✓			
Doo officia	_			
點選 OK 成功	輸出 Netlist			
	./inv.cir	×		
File Edit View Help	******	cādence		
<pre>* auCdl Netlist: * Library Name: Lab * Top Cell Name: inv * View Name: schematic * Netlisted on: Oct 2 15:46:41 2024</pre>				
.INCLUDE /RAID2/COURSE/vlsi_lab/vlsi_labTA01/AD4 *.BIPOLAR #.BFSI = 2000	<pre>FP/N16ADFP_iPDK/tsmcN16//Calibre/lvs/source.added</pre>			
* RESVAL * CAPVAL * DIOPERI + DIOADEA		Analysis Job	b Succeeded	
*.EQUATION *.SCALE METER *.MEGA .PARAM	Job '/RAI	, D2/COURSE/vlsi_lab/vlsi_labTA01/ADFP/N16ADFi	P_iPDK/' that was started at 'Oct 2 15:46:2	39 2024' has succ
* Library Name: Lab * Cell Name: inv * View Name: schematic		(<u>OK</u>) <u>C</u> an	icel <u>H</u> elp	
SUBOKT Inv I V00 V55 Z *.PININF0 II Z:0 V050 V558 MMm Z I V55 Snch_Jvt_mac l=16.0n nfin=12 m=1 MMp Z I V00 V00 pch_lvt_mac l=16.0n nfin=12 m=1 .ENOS				



3.4 複製輸出電路來模擬

- [~]\$ cd ~/ADFP
- [~/ADFP]\$ mkdir simulation

[~/ADFP] \$ cd simulation

[~/ADFP/simulation]\$ cp ~/ADFP/N16ADFP_iPDK/inv.cir.

```
DING! vlsi labTA01@cad11[~]$ cd ~/ADFP
16:00 vlsi labTA01@cad11[~/ADFP]$ mkdir simulation
16:01 vlsi_labTA01@cad11[~/ADFP]$ cd simulation
16:01 vlsi_labTA01@cad11[~/ADFP/simulation]$ cp ~/ADFP/N16ADFP_iPDK/inv.cir .
16:01 vlsi labTA01@cad11[~/ADFP/simulation]$
                                                                                                                                                                                                     simulation - File Manager
                  File Edit View Go Help

    A 
    A
    COURSE/vlsi_lab/vlsi_labTA01/ADFP/simulation/
    COURSE/vlsi_lab/vlsi_labTA01/ADFP/simulation/
    COURSE/vlsi_lab/vlsi_labTA01/ADFP/simulation/
    COURSE/vlsi_lab/vlsi_labTA01/ADFP/simulation/
    COURSE/vlsi_lab/vlsi_labTA01/ADFP/simulation/
    COURSE/vlsi_lab/vlsi_lab/vlsi_labTA01/ADFP/simulation/
    COURSE/vlsi_lab/vlsi_lab/vlsi_labTA01/ADFP/simulation/
    COURSE/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_vlsi_vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vlsi_lab/vl
                 DEVICES
                  画 File System
                  inv.cir
                 PLACES
                  ☆ vlsi_labTA01
                  Desktop
                  🗑 Trash
                  Documents
                  🛅 Music
                  Pictures
                  Videos
                  🛅 Downloads
                 NETWORK
                   🛒 Browse Netw.
註解以下欄位
                                                                                                                                                                                                                                                                    inv.cir
             Open 👻 🖪
                                                                                                                                                                                                                                                             ~/ADFP/s
           auCdl Netlist:
             Library Name: Lab
            Top Cell Name: inv
View Name: sch
            View Name: schematic
Netlisted on: Oct 2 15:46:41 2024
                                                                                                               *****
            .INCLUDE //RAID2/COURSE/vlsi_lab/vlsi_labTA01/ADFP/N16ADFP_iPDK/tsmcN16/../Calibre/lvs/source.added
              RTPOL
          *.RESI = 2000
            RESVAL
            . CAPVAL
           .DIOPERI
            DTOAREA
            . EQUATION
            .SCALE METER
            MEGA
           PARAM
            Library Name: Lab
             Cell Name:
                                              inv
            View Name:
                                               schematic
             *****
                                                                             *****
          .SUBCKT inv I VDD VSS Z
*.PININFO I:I Z<u>:O VDD:B VSS:B</u>
          Mn Z I VSS VSS
          MMp Z I VDD VDD
          ENDS
```



3.5 創建模擬環境

(1)新增一個檔案,這邊以 inv_tb.sp 為範例

File Edit View Go H	Help				
< > へ む	/RAID2/COU	JRSE/vlsi_lab/vlsi_labTA01//	ADFP/	/simulation/	
DEVICES File System thinclient_driv PLACES	inv.cir inv_1	tb.sp			
💮 vlsi_labTA01 🛅 Desktop 🎯 Trash		Create Folder Create Document	•	No templates installed	
Documents		Open Terminal Here Arrange Items	•	Empty File	
 Pictures Videos Downloads 		Zoom In Zoom Out Normal Size			
NETWORK		Properties			_

(1) Create new text file "inv_tb"

(2) 撰寫對應的 Test Bench

Library Path 如下,請記得 include 剛剛匯出的 pre-netlist (這邊是 inv.cir)

Library Path:

/ADFP/Executable_Package/Collaterals/Tech/SPICE/N16ADFP_SPICE_MODEL/n16ad fp_spice_model_v1d0_usage.l



(2) Completer Testbench Design



3.6 使用 Hspice 模擬

[~/ADFP/simulation]\$ hspice inv_tb.sp

*****	Runtime Statistics	s (seconds)	*****		
analysis	s time	# points	tot. iter	conv.iter	
op point	t 0.01	1	3		
transie	nt 0.02	10001	1111	452	rev= 79
readin	0.09				
errchk	0.08				
setup	0.01				
output	0.00				
	peak memory used	411.	.21 megabyte	S	
	total cpu time	Θ.	.20 seconds		
	total elapsed tim	ne 0.	.36 seconds		
	job started at	17:05:39	10/02/2024		
	job ended at	17:05:39	10/02/2024		
>info:	***** hspice	job conclud	ded		
	job total runtime	e 0.	.36 seconds		
	2				
lic: Rele	ease hspice token(s	5)			
lic: tota	al license che <u>ckou</u> t	elapse tim	ne: 0	.15(s)	
17:05 vls:	i labTA01@cad11[~//	DFP/simulat	tion]\$		
17:05 VIS:	L_tablA01@cadl1[~/#	ADFP/simulat	cion]\$		

simulate successfully

3.7 使用 WaveView 查看波型

[~/ADFP/simulation]\$ wv & 點選波形檔案(通常輸出為 *.tr0)

	Open : Waveform Files	×
File Tools Configuration		
Open Err Open Waveform Waveform Waveform Waveform	Path: simulation/ Sxcmd.log . inv.cir inv_tb.ic0 inv_tb.pa0 inv_tb.sp inv_tb.st0 inv_tb.st0	-
	File Name: inv_tb.tr0	1
	File Filter: All Files:*]
	Preload Waveforms to RAM	
	🗖 Read Multi-run Data as Multi-trace Waveform	
	Automatically Connect to Subsequent Split Files	
	🗖 x value shift offset:	
	🕀 🗖 Convert to WDF (compression)	-
	🕀 🗖 Load Data within Range Only	_
	Additional PWL/Table Format Options	_
	🗸 Ok O Apply 🤔 Help 🗙 Cancel	



3.8 點選欲觀察的訊號,即可查看波形

	Custom WaveView Version T-2022.06 Synopsys, Inc.	_ = ×
File Waveform Tools (onfiguration	2 🖬 🖓 🕻
Open Waveform Humo All Serren	Image: Sector of the sector	
WaveForm	₽ × waveview 1 ×	
Filter: (on toplevel)	🖸 🔍 🔍 🔍 🍭 🍳 🕇 🎟 🖄 🖗 工 🖮 ∿ 🤜 🗛 🗟 🗙 🗞	용 🖉 😫 🗸 🗴 🔍
Filter:▼ ▼ All € i(vvd) € i(vvin) € i(vvss) V(i) ♥ v(i) ♥ v(vd) ♥ v(vd) ♥ v(vd)	V(i) inv_tb 0.8 (int) 0.7 [±] 0.6 [±] 0.7 [±] 0.7 [±] 0.6 [±] 0.7 [±] 0.8 [±] (in)	
👰 v(z)	TIME(sec) (lin) 0 2n 4n 6n	8n 10n
		0%





4. Layout



4.2 Create Inverter Layout Design

請根據自行需求創建,可參考相關課程教學文件 COURSE05_VLSILAB_ADFP_layout_tutorial_2024-01-12.pdf



5. Layout Verification – DRC



(1) Create new folder for DRC



5.2 拷貝 DRC 規則

- Full-Chip Rule:
- [~/ADFP/DRC]\$ cp

/ADFP/Executable_Package/Collaterals/Tech/DRC/N16ADFP_DRC_Calibre/LOGIC_To pMr_DRC/N16ADFP_DRC_Calibre_11M.11_1a.encrypt ./

- Antenna Rule:
- [~/ADFP/DRC]\$ cp

/ADFP/Executable_Package/Collaterals/Tech/DRC/N16ADFP_DRC_Calibre/ANTENN A_DRC/N16ADFP_DRC_Calibre_11M_ANT.11_1a.encrypt ./

IP-Level Rule:

[~/ADFP/DRC]\$ cp /ADFP/Material/DRC/N16ADFP_DRC_Calibre_11M.11_1a.encrypt ./

一般課程範例建議使用 IP-Level Rule 避免出現一些可在 IP Level 忽略的 DRC · 例如: Density Check ·

	DRC - File Manager	×
File Edit View Go	Help	
< > へ 企	/RAID2/COURSE/vlsi_lab/vlsi_labTA01/ADFP/DRC/	G
DEVICES	Name Size Type	Date M
画 File System	N16ADFP_DRC_Calibre_11M.11_1a.encrypt 2.1 MiB C source code	Today
PLACES		
🎧 vlsi_labTA01	ADFP DRC Rule	
besktop		
🗑 Trash		
bocuments		
🛅 Music		
lictures		
🛅 Videos		
Downloads		
NETWORK		
🕎 Browse Network		
	1 item: 2.1 MiB (2,150,315 bytes), Free space: 132.3 TiB	

(2) Ensure that DRC rule is copied

如想更了解請參閱家目錄的浮水印文件,有關 DRC Rule 設定:

~/Desktop/ADFP_PDF/ADFP040_N16_DRC_Switch_Usage_wmp.pdf



5.3 從 Virtuoso 打開 Calibre







(4) 點選「Outputs」→ 勾選「Show results in RVE」→ 「Run DRC」



(3) Check DRC Result

Note: 因 ADFP 的 DRC 有加密,因此違反細節不會顯示在 RVE 當中

如想更了解請參閱家目錄的浮水印文件,有關 DRC Rule 說明:

~/Desktop/ADFP_PDF/ADFP039_N16ADFP_DRM_V1.1_1.pdf

善用 PDF 搜尋功能找到對應的 DRC 規則。



6. Layout Verification – LVS



(1) Create new folder for LVS



6.2 拷貝 LVS 規則

LVS Rule:

[~/ADFP/LVS]\$ cp -r /ADFP/Material/LVS ./

Rule file name: N16ADFP_LVS_Calibre



(2) Ensure whole directory is copied

如想更了解請參閱家目錄的浮水印文件,有關 LVS Rule 說明: ~/Desktop/ADFP_PDF/

ADFP003_N16_ADFP_Calibre_LVS_BOX_Command_Usage.pdf

ADFP004_N16_ADFP_Calibre_LVS_Deck_Usage.pdf

ADFP005_N16_ADFP_Dummy_Pickup_Checking.pdf

ADFP006_N16_ADFP_ERC_Usage.pdf

ADFP007_N16_ADFP_LOD_Measurement.pdf

ADFP008_N16_ADFP_LVS_Filter_Introduction.pdf

ADFP009_N16_ADFP_NF_MOS_Parallel_Reduction.pdf

ADFP010_N16_ADFP_STD_Filter_Cells.pdf

ADFP011_N16_ADFP_Unrecognized_Device.pdf



6.3 從 Virtuoso 打開 Calibre:

(1)點選「Calibre」→「Run nmLVS」→「Cancel」



(2) 點選「Rules」→「Load」→ 「選取剛剛複製過來的 LVS Rule」

Calibre Interactive - nmLVS v2019.2.26.18 _ ×
Bules Help Rules UNS Rules File
Rules LVS Rules File
/PATP2/COURSE/ulai lak/ulai lakTAD1/APED/US/CCT_ELOM/AUGADED_US/Calibaa
Inputs //RIDZ/COURDE/VISI_IAD/VISI_IAD/VISI_IAD/VISI/ED/VIO/COL_FLOW/NIORDFF_LV5_CALLDIE
Qutputs
Run Control
Transcript (/RAID2/COURSE/vlsi_lab/vlsi_labTA01/ADFP/LVS/CCI_FLOW
- Laver Derivations
Run LVS
Start RE (1) Fill and Check rule file and rup path
(1) Fill and Check fulle the and full path

(3)點選「Inputs」→「Layout」→ 勾選「Export from layout viewer」



(2) Check input layout



(4)點選「Inputs」→「Netlist」→ 取消勾選「Export from ... viewer」
(5)點選「Spice Files 旁的 View」→「選擇 Pre-sim 輸出的 sp 檔案」



(6) 點選「Outputs」→ 勾選「View Report after LVS finishes」→「Run LVS」

(7)查看 LVS 結果

		Calibre - RVE v2019.2_26	5.18 : svdb inv		-	۰	×
Eile View Highlight I	ools Window <u>S</u> etup H <u>e</u> lp						
🎾 🖋 🔍 🖉 👫 "	📡 🕵 🕴 Search	* < > _					
*Navigator **	Ma Extraction Results 80	omparison Results ×					
Results	Layout Cell / Type	Source Cell	Nets 4L 4S	Instances	Ports 4L 4S		
Comparison Result			,		,		
FRC ✓ ERC Results □ ERC Summary							
Reports	Coll in Summer (Clean)						
LVS Report	CELL IN Summary (Clean)	OMPARISON RESULTS (TOP	LEVEL)				13
Rules							
Rules File		ะ กุลกอนสอดแนนออน	1848				1
1 Info	(<i>*, *</i>	# CORRECT	₩Ţ,)			1
MFinder Schematics	"#"	äannaannaannaanna					
Setup							
@Options	LAYOUT CELL NAME: SOURCE CELL NAME:	inv inv					
	INITIAL NUMBERS OF OBJECTS	5					
		-				_	12 ¹⁴
							B

(5) Check LVS Result



7. Layout Verification – PEX



(1) Create new folder for PEX



7.2 拷貝 CCI_Flow 資料夾

[~/ADFP/PEX]\$ cp -r /ADFP/Material/CCI_FLOW ./

LVS Rule file name: N16ADFP_LVS_Calibre



7.3 從 Virtuoso 打開 Calibre LVS,產出 svdb 檔案:

(1)點選「Calibre」→ 「Run nmLVS」→ 「Cancel」

	\mathbf{U}								
Concurrent	Calibre Pegasus H	lelp			Calibre Ir	nteractive - nmLVS v2019	.2_26.18		_ = ×
_		<u> </u>	File Transcrip	pt <u>S</u> etup					Help
assic	Run nmDRC	Of	Rules	LVS F	hleg Rile	Load Runset File	×	View	Load
ect:0 Sel(NI):0	Run D <u>F</u> M		Qutputs	LUS	Runset File Path				
.cc.o Sei(iv).c	Run nmLVS		Run Control		Recent Punceto				
	Run PERC 2		Pup LIK	- E La					
	Run <u>P</u> EX		Start DUE						
	Run <u>x</u> ACT		Dear t Nys						
	Start <u>R</u> VE								
	Clear <u>H</u> ighlights				OK		Cancel		
2020 0350 2000	<u>S</u> etup						0		
	About						U		



(2) 點選「Rules」→「Load」→ 「選取剛剛複製過來的 LVS Rule」



(3)點選「Inputs」→「Layout」→ 勾選「Export from layout viewer」



(4)點選「Inputs」→「Netlist」→ 取消勾選「Export from ... viewer」

(5)點選「Spice Files 旁的 View」→「選擇 Pre-sim 輸出的 sp 檔案」

	Calibre Interactive - nmLVS v2019.2_26.18		-		×
File Transcrip	t <u>S</u> etup			Н	elp
Rules Inputs Qutputs Run Control	Run: Hierarchical Step: Layout vs Netlist Layout Netlist H-Cells Signatures Waivers				
Transcript	Format: SPICE - Export from	n schematic vi	ewer.	0	
Run <u>L</u> VS	Spice Files /RAID2/COURSE/vlsi_lab/vlsi_labTA01/ADFP/simulation/inv.c	ir ×	Vi	lew	
Start R <u>V</u> E	Top Cell: inv			8	
	Library Nam Lab		_		1
	View Name: schematic				1
	(3) Check input schematic				





(6)點選「Outputs」→ 勾選「View Report after LVS finishes」→ 勾選 「Generate Calibre Connectivity Interface Data」→「Run LVS」



(4) Generate CCI data for STARRC

(7)₫	查看 LVS	結果	2.5		
		Calibre - RVE v2019.2_26.18 : svdb in	v	_ = ×	
	Eile View Highlight 1	ools Window Setup Help			
	🖉 🖉 🔍 👘 🖉	X B Search			
	+Navigator) **	*≦ Extraction Results ● Comparison Results ×			
	Results	Layout Cell / Type Source Cell Nets	Instances Por S II. 1S 4L	ts	
	Contraction Result FRC Results FRC Results FRC Summary Fracts Fattaction Report CMS Reports Reports Rules Rules File View OInfo AFinder Ochematics Setup Options	Cell inv Sumary (Clean) Cell ComPARISON RESULTS (TOP LEVEL)			
		(5) Check LVS Re	sult		

7.4 使用 query_cmd 將 LVS 輸出檔轉為 StarRC 所需輸入檔

[~/ADFP/PEX/CCI_FLOW]\$ calibre -query ./svdb/ < query_cmd



7.5 針對欲抽取電路更改 star_cmd 與 pin_order.sp 內容



Modify "star_cmd" and "pin_order.sp"

_

Change Top Cell Name and Sub-Circuit Definition

7.6 根據 star_cmd 內容抽取寄生電路

[~/ADFP/PEX/CCI_FLOW]\$ StarXtract -clean star_cmd

	INITIATING HDB QUERY SERVER:						
	OK: Ready to serve.	Sotup	E10-00.00.05	Cpu-00.00.02	ller-2.2		Mom-400 0
	OK.	Secup	E(p=00:00:05)	Cpu=00:00:02	UST=2.3	Sys=0.0	Mem=409.0
	0K. 0K.	Models	E1p=00:00:00	Cpu=00:00:00	UST=0.5	Sys=0.0	Mom=409.1
	0K.	HN	E1p=00.00.00		llsr=0.0	Sys=0.0	$M_{OM} = 409.1$
_ /	0K. 0K.	DHETranslate	E1p=00.00.00	Cpu=00:00:00	llsr=0.0	Sys = 0.0	Mom-350 2
	ОК.	XrefHN	E1p=00:00:00	Cpu=00:00:00	llsr=0.0	Sys=0.0	Mem=358 2
	// Applying licensing policy	DHESort	E1p=00:00:00	Cpu=00:00:00	llsr=0.0	Sys=0.0	Mem=350.2
	// calibrexrc license acquired.	Cells	E1p=00.00.00	Cpu=00:00:00	llsr=0.0	Sys=0.0	Mem=409.1
1	(/incread_Draduate	Translate	Flp=00:00:00	Cpu=00:00:00	Usr=0.0	Sys=0.0	Mem=409.1
	// Licensed Products	BulkLaverHandling	Flp=00:00:00	Cpu=00:00:00	Usr=0.0	Sys=0.0	Mem=356.0
	<pre>// Base products running on 1 core:</pre>	DetectDirection	Elp=00:00:00	Cpu=00:00:00	Usr=0.0	Svs=0.0	Mem=350.2
	<pre>// - Calibre Connectivity Interface // Other products:</pre>	XtractPreP-Resbody	Elp=00:00:01	Cpu=00:00:00	Usr=0.0	Svs=0.1	Mem=508.4
	// - Query Server	NetlistSetup	Elp=00:00:00	Cpu=00:00:00	Usr=0.0	Svs=0.0	Mem=350.2
	OK.	GPD XtractSetup	Elp=00:00:00	Cpu=00:00:00	Usr=0.0	Svs=0.0	Mem=409.1
	OK.	GPD Instance Setup	Elp=00:00:00	Cpu=00:00:00	Usr=0.0	Sys=0.0	Mem=350.2
	0К.	GPD NameMap	Elp=00:00:00	Cpu=00:00:00	Usr=0.0	Sys=0.0	Mem=350.7
	OK.	xTract	Elp=00:00:13	Cpu=00:00:12	Usr=10.1	Sys=2.1	Mem=3001.6
	0K.	GPD Instance	Elp=00:00:00	Cpu=00:00:00	Usr=0.0	Sys=0.0	Mem=350.2
<u>۱</u>	0K.	xTractPP	Elp=00:00:00	Cpu=00:00:00	Usr=0.0	Sys=0.0	Mem=256.4
1	ок.	ReportViolations	Elp=00:00:00	Cpu=00:00:00	Usr=0.0	Sys=0.0	Mem=350.2
	0K.	GPD_PostProcess	Elp=00:00:00	Cpu=00:00:00	Usr=0.0	Sys=0.0	Mem=350.2
· \	OK.	GPD_CouplingReport	Elp=00:00:00	Cpu=00:00:00	Usr=0.0	Sys=0.0	Mem=350.2
· \	0K.	GPD_Converter1	Elp=00:00:00	Cpu=00:00:00	Usr=0.0	Sys=0.0	Mem=255.5
	0K. 0K.	GPD_Converter2	Elp=00:00:00	Cpu=00:00:00	Usr=0.0	Sys=0.0	Mem=255.5
	ОК.	<pre>GPD_Converter_Instance</pre>	Elp=00:00:00	Cpu=00:00:00	Usr=0.0	Sys=0.0	Mem=255.5
	OK.	GPD_Converter_merge	Elp=00:00:00	Cpu=00:00:00	Usr=0.0	Sys=0.0	Mem=255.4
	0						
	OK. OK: Teminating.	Done Elp=00:00	0:19 Cpu=00:00	9:14 Usr=12. <u>7</u>	Sys=2.2	Mem=3001	.6
			•				
	Owner Descript		S	tar-RC F	kesult		
	Query Result						

Advanced IC Lab

7.7 查看 Extract 出的寄生電路

File Edit View Go	Help		Open 👻 🖪		Save	= ×	4
$\langle \rangle \land \hat{\omega}$	/RAID2/COURSE/vlsi_lab/vlsi_labTA01/ADFP/PEX/CCI_FLOW/	1	1 *	-month Execution			
DEVICES	Name		2 * DSPF 1.3 3 * DESIGN inv	* 14 15-24-00 2024			
画 File System	🛅 svdb		5 * VENDOR "Synop	opsys"			
🚐 thinclient_driv ≙	TAR_MAP		6 * PROGRAM "Star 7 * VERSION "0-20	arRC" 2019.12-SP5-3"			
PLACES	a star		8 * DIVIDER /				
	inv.gpd		10 **FORMAT SPF				
Deskton	DFM		11 * 12				
Sesktop	E tech_file		13 ** COMMENTS				
irash	star_cmd		15 ** OPERATING_TE	TEMPERATURE 25			
Documents	📄 query_cmd		16 ** DENSITY_OUTS 17 ** GLOBAL TEMPE	ISIDE_BLOCK 0 PERATURE 25			
Music	PIPO.SUM.inv		18 **				
Pictures	PIPO.LOG.inv		N16ADFP_STARRC	LLE /ADFP/Executable_Package/Collaterals/Tech/RC/N16ADFP_STAR	(C/		
🛅 Videos	pin_order.sp		20 ** TCAD_TIME 21 ** TCADGRD VE	_ STAMP Wed Feb 16 13:17:27 2022 /FRSION 84			
Downloads	pin_file.txt		22 22 CUDCKT inv VC				
NETWORK			23 .SUBCKT THV VS:	55 2 000 1			
🛒 Browse Netw	N16ADFP_LVS_Calibre		25 26				
	inv.star_sum		27				
(inv.spf		29				
	inv co	1	30				
	inv.lvs.report.ext		32				
	inv.lvs.report		34				
	inv.calibre.db		35 36 7 Pto 117-Pto	10			
	CCI_DB.ports_cells			Plain Text 👻 Tab Width: 8 👻	Ln 1, Col 1		5
		-					_

Extracted Netlist





8. Post-Layout Simulation



8.1 複製 Layout 產生的 spice 檔案

[~] \$ cd ~/ADFP/simulation

[~/ADFP/simulation]\$ cp ~/ADFP/PEX/CCI_FLOW/inv.spf ./

r	sim	ulation - File M	anager	_ = ×					
File Edit View Go	File Edit View Go Help								
< > へ 企	/RAID2/COURSE/	vlsi_lab/vlsi_lab	TA01/ADFP/simulation/	G					
DEVICES	Name	▲ Size	Туре	Date Modified					
画 File System	sxcmd.log.3	4.8 KiE	3 MATLAB script/function	10/02/2024					
📖 thinclient_driv 🚔	sxcmd.log.2	839 bytes	MATLAB script/function	10/06/2024					
PLACES	sxcmd.log.1	870 bytes	MATLAB script/function	10/06/2024					
	sxcmd.log	597 bytes	application log	10/06/2024					
	inv_tb.tr0	16.7 Ki	3 unknown	10/02/2024					
	inv_tb.st0	4.4 KiE	3 plain text document	10/02/2024					
l rash	inv_tb.sp	434 bytes	differences between files	10/02/2024					
Documents	inv_tb.pa0	15 bytes	plain text document	10/02/2024					
🛅 Music	inv_tb.ic0	499 bytes	plain text document	10/02/2024					
🛅 Pictures	inv.spf PO	st-Sim	pa Netwet t	Today					
🛅 Videos	inv.cir Pr	50 byte:	hinter document	10/02/2024					
bownloads		C-0111	Nethot						
NETWORK									
🕮 Browse Netw									
	11 items: 46.4 KiB (4	7,482 bytes), Fr	ee space: 132.3 TiB						



8.2 修改 TestBench include 的 netlist

	Open 👻	æ		inv_tb.: ~/ADFP/simu	SP lation			Save	≡	×
1	*** Inve	erter	Testbench ***							
3	.op	post								
4	.TEMP 25	5.0								
6	** Libra	ary								
7	.LIB "/F	AID2	/PROCESS/ADFP/Exec	utable_Package/Coll	aterals/Te r∆p	ch/SPICE/N16ADF	P_SPIC	E_MODEL	-/	
8	intoudry	opre	e_modee_vide_dodge		cru					
19	** Inclu	ide Y	our Circuit							
11	.include		inv.spf"							
12										
14	xinv i v	/dd v	ss z inv							
10	0 7 VC	: 10e	- 15							
17	** Sourc	e								
18	vvss vs	6 O D	C=0							
20	vvaa vaa vvin i G	D D D D D D D D D D D D D D D D D D D	C=0.8 SE(0 0.8 0 10p 10p	480p 1000p)						
21										
22	.TRAN 1	/SIS 0 10n								
24										
25	. END									
	ľ									
					DICC					

Modify Testbench Design

8.3 修改並確認 TestBench 呼叫電路時的 Pin 的順序與 netlist 一致



Check Pin Order



8.4 跑 Hspice simulation

[~/ADFP/simulation]\$ hspice inv_tb.sp -hpp -mt 4

*****	Runtime	Statistics	(s	econds)	**	****	*					
analysis		time	#	points	to	ot.	iter	conv.i	ter			
op point		0.02		1			16					
transien	t	0.05		10001			729		340	rev=	20	
readin		0.09										
errchk		0.09										
setup		0.02										
output		0.00										
	neek m	monu used		411	60		abuta	~				
	peak me	emory used		411.	09	meg	abyte	5				
	totat	cpu time		0.	21	sec	onas					
	total	etapsed time	۰.	5 40 07	44	sec	onds					
	job sta	arted at	1	5:40:07	10,	14/	2024					
	job end	ded at	1	5:40:07	10,	/14/	2024					
>info:		*** hspice	iob	conclu	led							
	job tot	tal runtime		Θ.	.44	sec	onds					
lic: Rele	ase hsp	ice token(s										
lic: tota	1 licens	se checkout	el	anse tim	le:		Θ	.17(s)				
15:40 vlsi	labTAO	1@cad11[~/A	FP	/simulat	in	115						
19110 1031		recourt[//		- samu cur	101	.,						
	simulato successfully											

當電路比較大時,而為了縮減模擬檔案內容進而節省個人 (組群) 的硬碟空間,請 務必於 Hspice Testbench 當中輸入檔中先啟用 .option post=2 probe print 功 能,再利用 .probe 或 .print 設定所需要的訊號或資訊即可。

Hspice 電路模擬的補充說明:

為縮減所產生的模擬檔, Hspice 檔案內鍵入 .option post=2 probe print 設定 以儲存必要輸出之模樣結果 (最多兩層的結果)。

```
.OPTION
POST=n Saves results for viewing by an interactive waveform viewer. Default is 0.
PROBE=n Limits post-analysis output to only variables specified in .PROBE and .PRINT
statements. Default is 0.
```

並利用 .probe 與 .print 指令,選取必要輸出的模擬結果,以減少模擬輸出結果 檔案大小。

.print test='V (VS) /abs (I (mm1)) '

```
.probe test='V ( VS ) /abs ( I ( mm1 )) '
```

.print 結果會在.list 檔內(.lis) .probe 結果以 waveform (.tr0)呈現

.print: Prints numeric analysis results in the output listing file (and post-

processor data if .OPTION POST is used) .

.probe: Outputs data to post-processor output files but not to the output listing (used with .OPTION PROBE to limit output).

參考資料: <u>HSPICE: Quick Reference</u> | <u>HSPICE: User Guide, Simulation and Analysis</u> | <u>HSPICE: Reference</u>
 <u>Manual</u>



如果電路龐大可使用平行運算功能,Hspice 提供兩種平行運算機制:

(1)本機單工多緒機制 (-mt,適用單一模擬工作)。

- ▶ 在此模式下 Hspice 利用多緒做加速運算,故需 N 個 CPU core。
- ▶ 指令範例: hspice inv_tb.sp -mt N
- ▶ 建議加上參數 hpp (high performance parallel),效果更好
- ▶ 指令範例: hspice inv_tb.sp -mt N -hpp

(2)本機多工多緒機制 (-mp 加 -mt,但 overhead 較重)。

當使用 ALTER 可拆成多個多緒子工作,共需 N x M 個 CPU core。
 .param supply = 1.8v
 .alter
 .param supply = 2v
 .alter
 .param supply = 1.6v 共需跑三次,此時用-mp 3 會有顯著效果。
 指令範例: hspice test.sp -mp M -mt N -hpp

Hspice 平行運算效益案例 (藍色為使用 alter 共跑 3 次的檔案模擬):

平行運算機制	使用的 core	實際使用率	執行時間	平行運算的效益
無	1	98%	12:03	1 X
-mt 2	2	198%	13:22	0.9 X
-mt 4	4	396%	11:47	1.02 X
-mt 4 -hpp	4	387%	03:52	3.12 X

平行運算機制	使用的 core	實際使用率	執行時間	平行運算的效益
無	1	99%	36:10	1 X
-mt 4 -hpp	4	390%	12:21	2.93 X
-mp 3 -mt 4 -hpp	12	99% (主線程)	04:29	8.07 X

Note: 請盡量不要超過 -mt4 避免資源的佔用,使用時搭配 -hpp 效果更好。



8.5 使用 WaveView 查看波型

[~/ADFP/simulation]\$ wv &

File Tools Configuration	Open : Waveform Files	·×	×
Image: Tools Colinguistor Image: Tools Colinguistor Image: Tools Image: Tools Image: Tools	Path: simulation/	F	
	File Name: inv_tb.tr0 File Filter: All Files:* Image: Preload Waveforms to RAM Read Multi-run Data as Multi-trace Wave Image: Preload Waveforms to RAM Read Multi-run Data as Multi-trace Wave Image: Preload Waveforms to Subsequent S Image: Preload Waveforms to Subsequent S Image: Preload Waveforms to Subsequent S Image: Preload Waveforms to Subsequent S Image: Preload Waveforms to WDF (compression) Image: Preload Waveforms Image: Preload Waveforms to WDF (compression) Image: Preload Waveforms Image: Preload Waveforms to WDF (compression) Image: Preload Waveforms Image: Preload Waveforms Image: Preload Waveforms Image: Preload W	eform plit Files	

8.6 點擊欲察看訊號,比較 Pre-sim 和 Post-sim 差異。





9. 查看 TSMC 提供之 FC 文件範例練習

請參閱家目錄的浮水印文件,有關 FC 說明: ~/Desktop/ADFP_PDF/

(1) ADFP046_TSMC_N16ADFP_Introduction_20220118_wmc.pdf

有關 TSMC ADFP 製程的簡要說明。

(2) ADFP044_TSMC_N16ADFP_Layout_20220118_wmc.pdf

有關 2D-Planner 和 FinFET Layout 的理論介紹和差異(圖解)

以及特別的 DRC Rule 和 Layer 層說明。

(3) ADFP042_TSMC_N16ADFP_Lab_Layout_20220211_wmc.pdf

該文件提供 Lab 練習,使用 Layout Tool 繪製基本邏輯閘。

(4) ADFP047_TSMC_N16ADFP_SPICE_20220118_wmc.pdf

有關 Spice model 的說明。



10. 查看 NYCU 課程提供之 FC 文件範例練習

請參閱家目錄的浮水印文件,有關 FC 說明: ~/Desktop/ADFP_PDF/

(1) COURSE04_VLSILAB_ADFP_full_custom_tutorial_2024-01-12.pdf

有關 TSMC ADFP 製程的簡要說明。有關 2D-Planner 和 FinFET Layout 的理論介紹 和差異(圖解)以及特別的 DRC Rule 和 Layer 層說明。

(2) COURSE05_VLSILAB_ADFP_layout_tutorial_2024-01-12.pdf

有關如何「善用」ADFP 各層來實現 AOI 數位邏輯閘。





Revision Record and Author List

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